REMARKS

The drawings are amended for reasons specified in the Office Action at page 2, section 2. Specifically, the legend "PRIOR ART" is added in Figure 1 of the drawings.

Claims 18-20 are rejected under 35 U.S.C. § 112, second paragraph, as being indefinite. Claim 18 is amended above in a manner believed to overcome the rejection. Entry of the amendment to claim 18 and removal of the rejection are respectfully requested.

Claims 1-20 are rejected under 35 U.S.C. 102(e) as being anticipated by Miyazaki (United States Publication No. 2002/0154080). In view of the amendments to the claims and the following remarks, it is believed that the amended claims are allowable over the cited references.

The present invention as claimed in amended independent claim 1 is directed to a liquid crystal display driver comprising a driving voltage generating circuit 21, a common/segment driving circuit 23, a first capacitor C5, a second capacitor C6, a third capacitor C7, and a control circuit 25. The control circuit comprises a plurality of switches 251-254 for controlling connection of output terminals and the capacitors in response to a driving polarity signal CON. Each switch 251-254 is controlled by the driving polarity signal CON.

The present invention as claimed in independent claim 10 is further directed to a first switch 251 for connecting one end of a second capacitor C6 to one of a first output terminal (at first driving voltage) V0 and a fifth output terminal (at fifth driving voltage V4) in response to a driving polarity signal CON. A second switch 252 connects the other end of the second capacitor C6 to one of a second output terminal (at second driving voltage V1) and ground voltage VSS in response to the driving polarity signal CON. A third switch 253 connects one end of a third capacitor C7 to one of the second output terminal and a fourth output terminal (at fourth driving voltage V3) in response to the driving polarity signal CON. A fourth switch 254 connects the other end of the third capacitor C7 to one of a third output terminal (at third driving voltage V2) and the fifth output terminal in response to the driving polarity signal.

The present invention as claimed in amended independent claim 18 is directed to a method for reducing a number of capacitors for driving voltage stabilization in a liquid crystal display driver. A first capacitor C5 is connected between a first output terminal (at V0) and a ground voltage VSS. When a driving polarity signal CON is in a first logic state, one end of a

second capacitor C6 is connected to a fifth output terminal (at V4) by a first switch 251, the other end of the second capacitor C6 is connected to the ground voltage VSS by a second switch 252, one end of a third capacitor C7 is connected to a fourth output terminal (at V3) by a third switch 253, and the other end of the third capacitor C7 is connected to the fifth output terminal (at V4) by a fourth switch 254. When the driving polarity signal CON is in a second logic state, one end of the second capacitor C6 is connected to the first output terminal (at V0) by the first switch 251, the other end of the second capacitor C6 is connected to the second output terminal (at V1) by the second switch 252, one end of the third capacitor C7 is connected to the second output terminal (at V1) by the third switch 253, and the other end of the third capacitor C7 is connected to the third output terminal (at V2) by the fourth switch 254.

The claims are amended herein to clarify certain details of the present invention. Specifically, claim 1 is amended to clarify that each switch of a plurality of switches is controlled by a driving polarity signal.

With regard to amended independent claim 1, it is submitted that Miyazaki fails to teach or suggest each switch of a plurality of switches being controlled by a driving polarity signal, as claimed in amended independent claim 1. Instead, Miyazaki discloses in a first embodiment a first switch SW1 and a second switch SW2 (see Miyazaki, Figure 5). Miyazaki further discloses in the first embodiment a frame signal (referred to in the Office Action at page 3, section 8 as a driving polarity signal) and a separate clock signal CLK0, wherein the clock CLK0 is generated at the same timing as the frame signal (see Miyazaki, Figures 5-6 and page 4, paragraph [0060]). The second switch SW2 of Miyazaki is controlled by the clock CLK0 (see Miyazaki, Figures 5-6 and page 4, paragraph [0060]). However, the first switch SW1 of Miyazaki is controlled by another clock CLK1 or a clock obtained by dividing the other clock CLK1 (see Miyazaki, Figure 6 and page 5, paragraph [0062]). Thus, neither the first switch SW1 nor the second switch SW2 is controlled by the frame signal FR. In another embodiment, as shown in Figures 9-10 of Miyazaki, a first clock CLK(SW1) is applied to a first switch SW1, a second clock CLK(SW2) is applied to a second switch SW2, and a third clock CLK(SW3) is applied to a third switch SW3. While this embodiment likewise discloses a frame signal FR, there is no mention of the frame signal FR controlling either the first switch SW1, second switch SW2, or third switch SW3. In the embodiments described above, as well as the other embodiments described in Miyazaki, the

switches of Miyazaki are not controlled by a driving polarity signal, but are instead controlled by clock signals that are independent of a frame signal. There is no mention in Miyazaki of each switch SW1, SW2, SW3 of Miyazaki being controlled by a driving polarity signal, as claimed. Moreover, the Miyazaki does not apply the same clock signal to each of the switches of Miyazaki. For example, in Figure 10, Frame 1 of Miyazaki, Frame Signal and CLK(SW1) are in a logic low position, wherein clock signal CLK(SW1) is applied to switch SW1, which appears to be a similar clock signal as the frame signal FR. However, clock signal CLK(SW2) is a different clock signal than clock signal than clock signal CLK (SW1). Since the switches SW1, SW2 are each controlled by a different clock signal, and since neither clock signal is the frame relay signal FR, it follows that the switches of Miyazaki are not the Applicant's claimed switches.

With regard to independent claim 10, it is submitted that Miyazaki fails to teach or suggest a first switch for connecting one end of a second capacitor to one of a first output terminal and a fifth output terminal in response to a driving polarity signal, as claimed. Instead Miyazaki teaches a switch SW3 that connects one end of a capacitor C4 to ground [when switch SW3 is in position a] or to voltage level V1 [when switch SW3 is in position b] (see Miyazaki, Figure 8). However, the other end of the capacitor C4 is directly coupled to voltage level V5(V2), regardless of the switch SW3 position. Since one end of the capacitor C4 can optionally be connected to the voltage level V1 and the other end of the capacitor C4 is directly coupled to the voltage level V5(V2), it follows that the switch SW3 of Miyazaki is not a first switch, as claimed in claim 10.

In addition, it is submitted that Miyazaki fails to teach or suggest a second switch for connecting another end of a second capacitor to one of a second output terminal and a ground voltage in response to a driving polarity signal, as claimed. In Miyazaki, when switch SW2 is in position b, the other end of capacitor C4 is connected to voltage node V82, and when switch SW2 is in position a, the other end of capacitor C4 is connected to voltage node V85. The Office Action at page 3, section 8 refers to voltage levels V2 and V5 as being second and fifth terminals. As such, there is no switch between the other end of capacitor C4 and voltage level V5(V2). Further, there is no mention in Miyazaki of the switch SW2 connecting the other end of capacitor C4 to a ground voltage. Instead, switch SW3 connects one end of the capacitor C4 to

ground (see Miyazaki, Figure 8). For these reasons, it therefore follows that switch SW2 of Miyazaki is not a second switch, as claimed in claim 10.

In addition, it is submitted that Miyazaki fails to teach or suggest a third switch for connecting one end of a third capacitor to one of a second output terminal and a fourth output terminal in response to a driving polarity signal, as claimed in claim 10. Miyazaki teaches a switch SW1 (referred to in the Office Action at page 4, line 10 as a third switch) and a capacitor C3 (referred to in the Office Action at page 4, line 3 as a third capacitor). The switch SW1 of Miyazaki connects one end of the capacitor C3 to one of a voltage level V4 (referred to in the Office Action at page 3, section 8 as a fourth driving voltage) and a voltage level V3 (referred to in the Office Action at page 3, section 8 as a third driving voltage). There is no mention in Miyazaki of the switch SW1 connecting capacitor C3 to one of a second output terminal and a fourth output terminal in response to a driving polarity signal, as claimed in claim 10. It therefore follows that switch SW1 of Miyazaki is not the third switch, as claimed in claim 10.

In addition, it is submitted that Miyazaki fails to teach or suggest a fourth switch for connecting another end of a third capacitor to one of a third output terminal and a fifth output terminal in response to a driving polarity signal, as claimed in claim 10. The Office Action at page 4, first paragraph, refers to switch SW3 in position b as being a first switch, switch SW2 in position b as being a second switch, and switch SW1 in position a as being a third switch. However, if switches SW1, SW2, and SW3 are considered to be analogous to a first switch, second switch, and third switch, as asserted, then Miyazaki would have no analog of a fourth switch, as claimed. While the Office Action at page 4, first paragraph, further asserts that switch SW2 in position a of Miyazaki is a fourth switch, it is submitted that, if switch SW2 is considered to be a fourth switch, as claimed, then Miyazaki would have no analog of a second switch, as claimed. Moreover, there is no mention in Miyazaki that switch SW2 in position a connects another end of a third capacitor to one of a third output terminal and a fifth output terminal in response to a driving polarity signal, as claimed in claim 10.

With regard to amended independent claim 18, it is submitted that Miyazaki fails to teach or suggest that when the driving polarity signal is in a first logic state, connecting one end of a second capacitor to a fifth output terminal by a first switch, connecting another end of a second capacitor to a ground voltage by a second switch, connecting one end of a third capacitor to a

fourth output terminal by a third switch, and connecting another end of the third capacitor to the fifth output terminal by a fourth switch, as claimed, for reasons similar to those described above.

In addition, it is submitted that Miyazaki fails to teach or suggest that when a driving polarity signal is in a second logic state, connecting one end of a second capacitor to a first output terminal by a first switch, connecting another end of the second capacitor to asecond output terminal by a second switch, connecting one end of a third capacitor to a second output terminal by the third switch, and connecting another end of a third capacitor to a third output terminal by a fourth switch, as claimed, for reasons similar to those described above.

For these reasons, it is submitted that Miyazaki fails to teach or suggest the present invention, as claimed. Reconsideration and removal of the rejection of claims 1-20 under 35 U.S.C. 102(e) based on Miyazaki are respectfully requested.

In view of the amendments to the claims and the foregoing remarks, it is believed that all claims pending in the application are in condition for allowance, and such allowance is respectfully solicited. If a telephone conference will expedite prosecution of the application, the Examiner is invited to telephone the undersigned.

Respectfully submitted,

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Mills & Onello, LLP
Eleven Beacon Street, Suite 605
Boston, MA 02108
Telephone: (617) 994-4900
Facsimile: (617) 742-7774
J:\SAM\0437\amenda\amendmenta.wpd

Steven M. Mills
Registration Number 36,610
Attorney for Applicants

Annotated Sheet Showing Changes

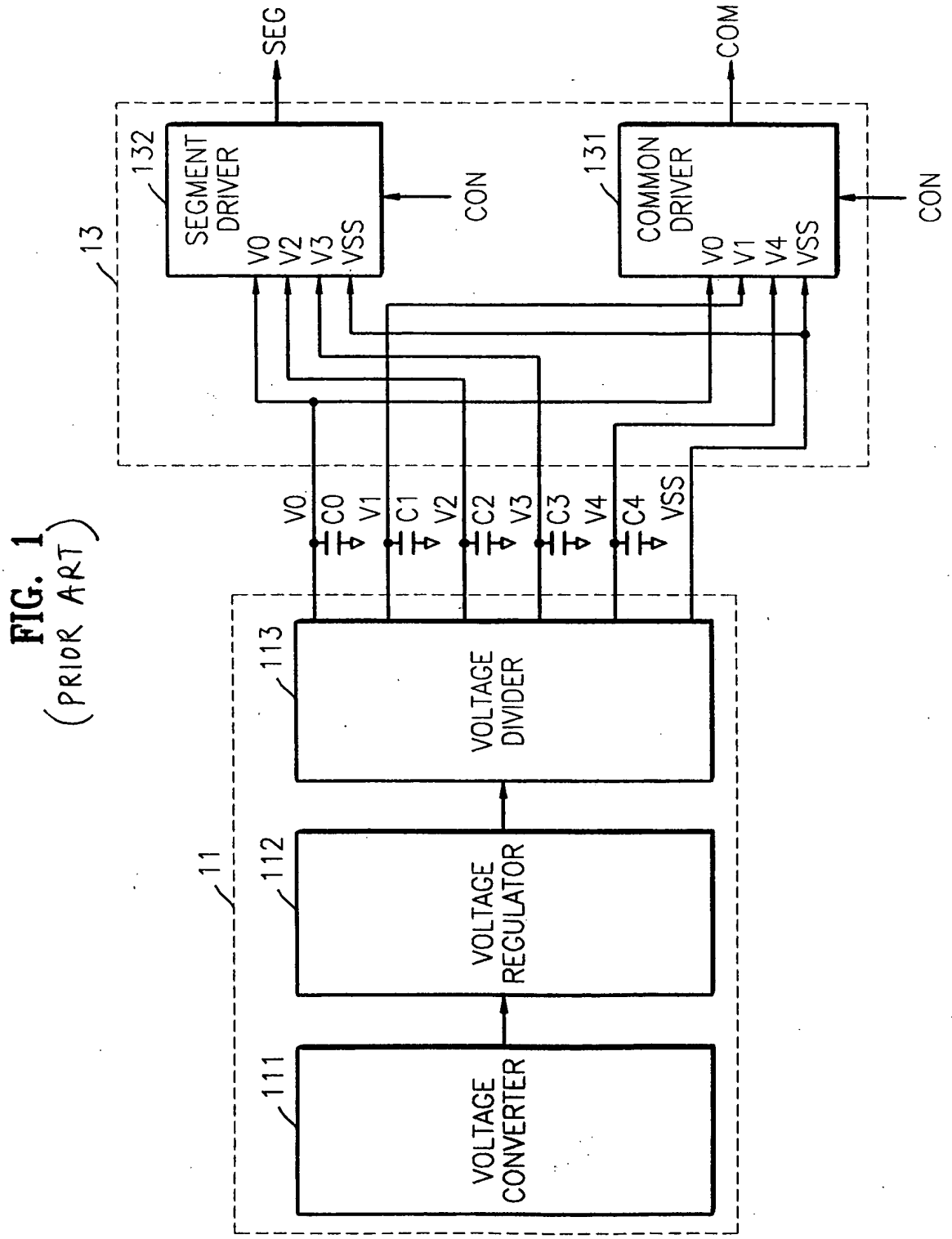

FIG. 1
(PRIOR ART)